Apr. 2023

SemiHow
Know-How for Semiconductor

HCD90R800

900V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)}$ X Q_g)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

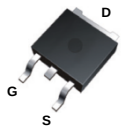
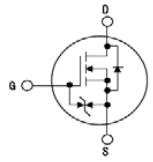
Key Parameters

Parameter	Value	Unit
BV_{DSS} @$T_{j,max}$	950	V
I_D	6.7	A
$R_{DS(on),\ max}$	0.8	Ω
$Q_{g,\ Typ}$	17.4	nC

Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV power & LED Lighting Power
- AC to DC Converters
- Telecom

Package & Internal Circuit

D-PAK	SYMBOL
	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	900	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current - Continuous (T_C = 25℃)	6.7	A
	Drain Current - Continuous (T_C = 100℃)	4.2	A
I_{DM}[1)]	Drain Current - Pulsed	20	A
E_{AS}[2)]	Single Pulsed Avalanche Energy	83	mJ
I_{AR}	Avalanche Current	1.40	A
dv/dt	MOSFET dv/dt ruggedness, VDS=0…400V	50	V/ns
dv/dt	Reverse diode dv/dt, V_{DS}=0…400V, I_{DS}≤I_D	15	V/ns
P_D	Power Dissipation (T_C = 25℃)	78	W
$T_{J,}$ T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{θJC}$	Thermal Resistance, Junction-to-Case, Max.	1.6	℃/W
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient , Max.	62.5	℃/W

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Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 280 μA	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.7 A	-	0.696	0.8	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1mA	900	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 900 V, V_{GS} = 0	-	-	1	μA
		V_{DS} = 900 V, T_C = 150℃	-	-	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 500 V, V_{GS} = 0 V, f = 1.0 MHz	-	740	-	pF
C_{oss}	Output Capacitance		-	15	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.8	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 450 V, I_D = 3.6 A, R_G = 25 Ω (Note 3,4)	-	23	-	ns
t_r	Turn-On Rise Time		-	20	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	91	-	ns
t_f	Turn-Off Fall Time		-	17	-	ns
$Q_{g(}$	Total Gate Charge	V_{DS} = 720 V, I_D = 3.6 A, V_{GS} = 10 V (Note 3,4)	-	17.4	-	nC
Q_{gs}	Gate-Source Charge		-	3.2	-	nC
Q_{gd}	Gate-Drain Charge		-	5.5	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	6.7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	20	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.6 A	-	-	1.3	V
trr	Reverse Recovery Time	V_R = 400 V, I_F = 3.6 A, di_F/dt = 100 A/μs	-	278	-	ns
Qrr	Reverse Recovery Charge		-	2.3	-	μC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=1.40A V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
4. Essentially Independent of Operating Temperature

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Typical Characteristics

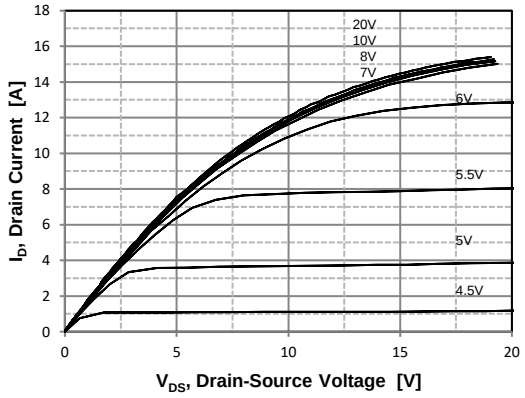

Figure 1. On Region Characteristics

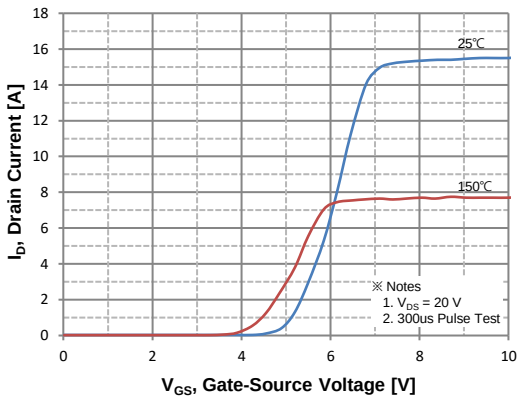

Figure 2. Transfer Characteristics

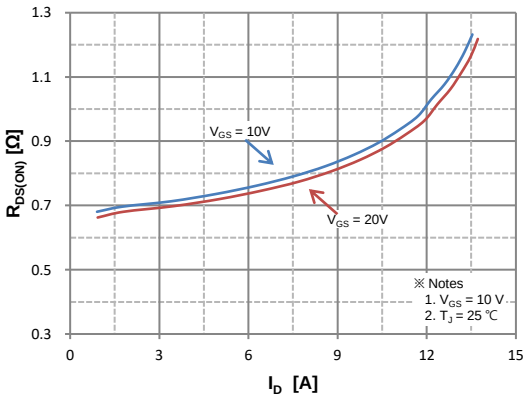

Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

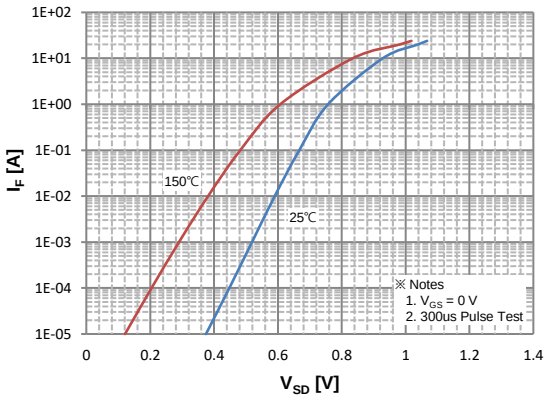

Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

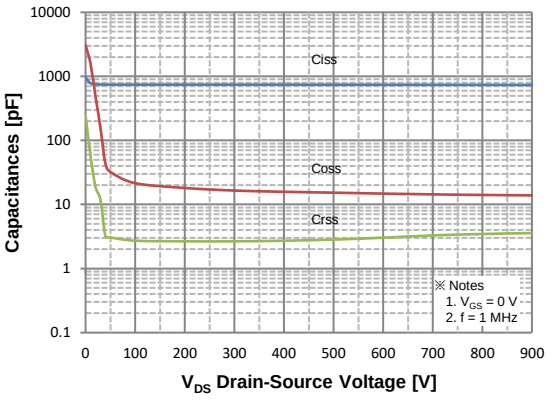

Figure 5. Capacitance Characteristics

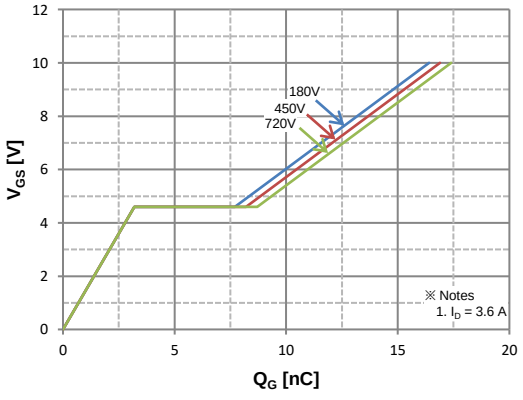

Figure 6. Gate Charge Characteristics

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Typical Characteristics

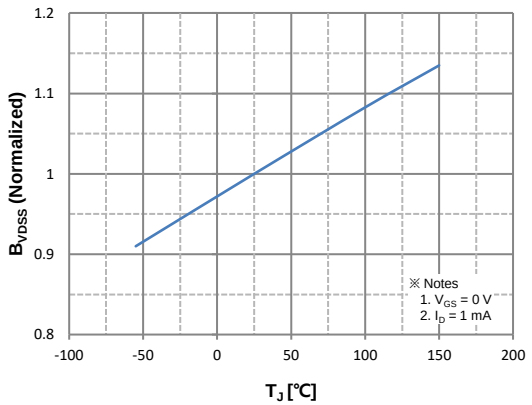

Figure 7. Breakdown Voltage Variation vs. Temperature

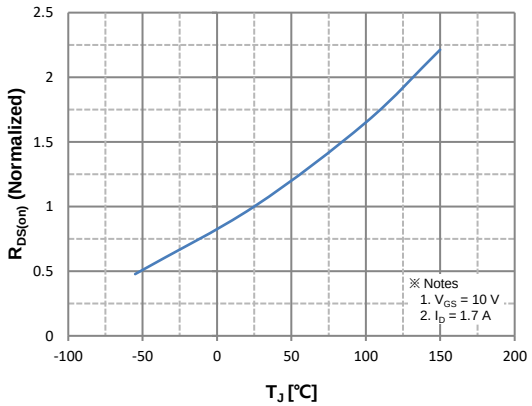

Figure 8. On-Resistance Variation vs. Temperature

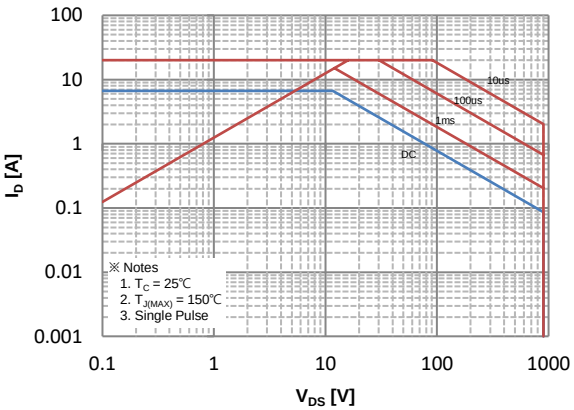

Figure 9. Maximum Safe Operating Area

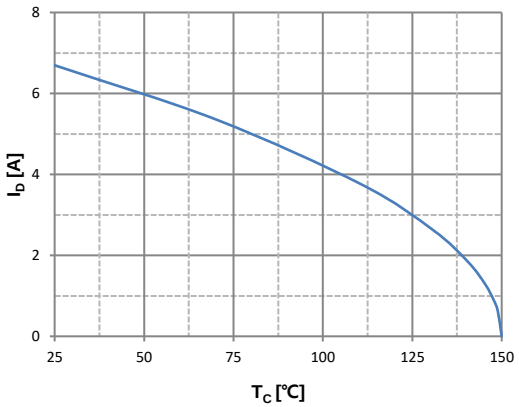

Figure 10. Maximum Drain Current vs. Case Temperature

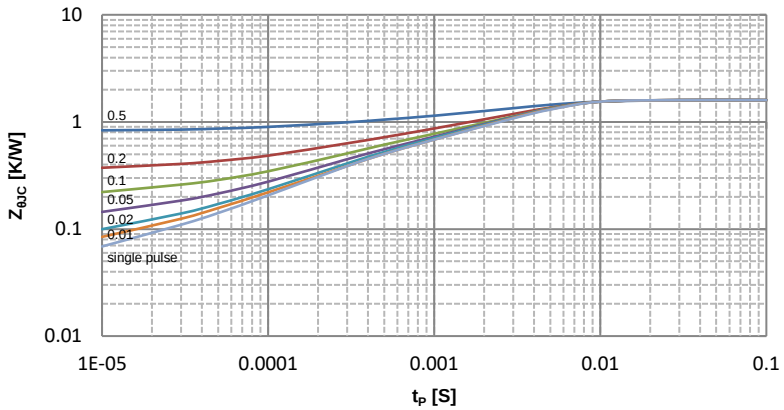

Figure 11. Transient Thermal Response Curve

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Fig 12. Gate Charge Test Circuit & Waveform

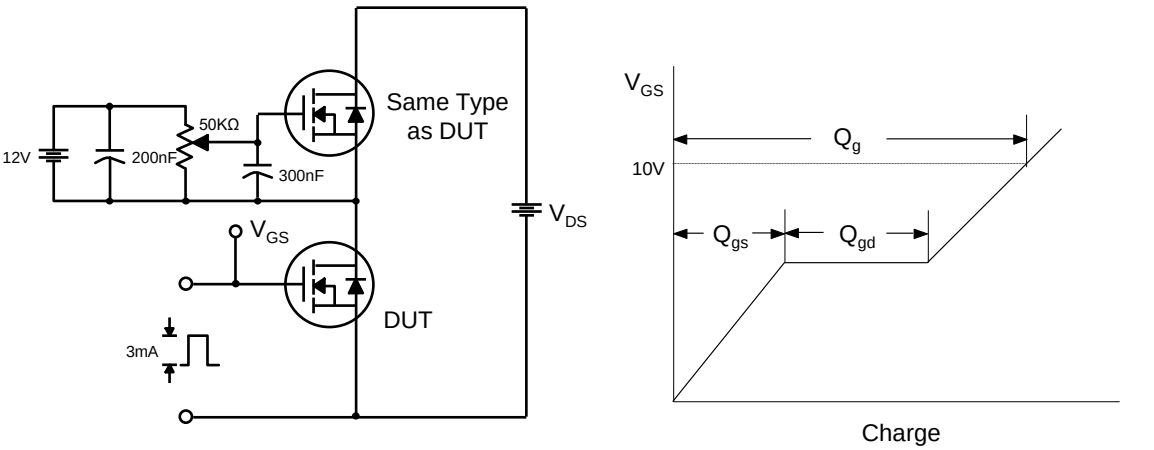

Fig 13. Resistive Switching Test Circuit & Waveforms

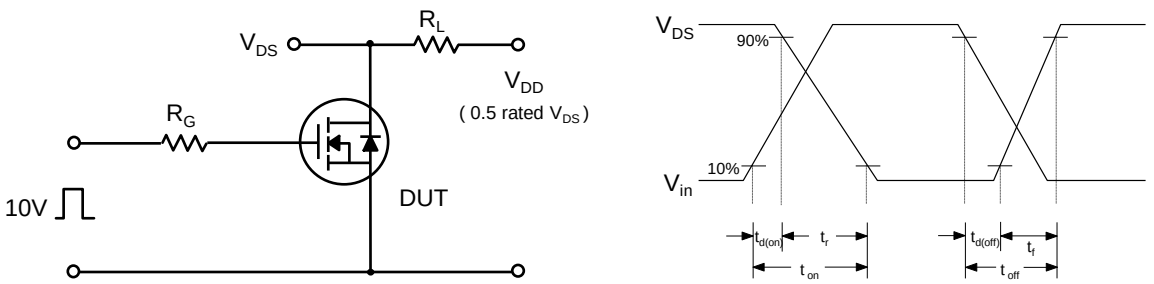

Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

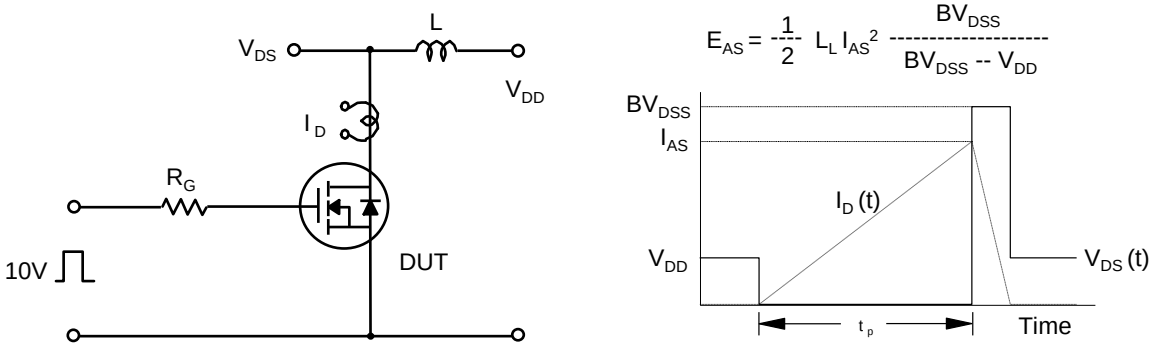

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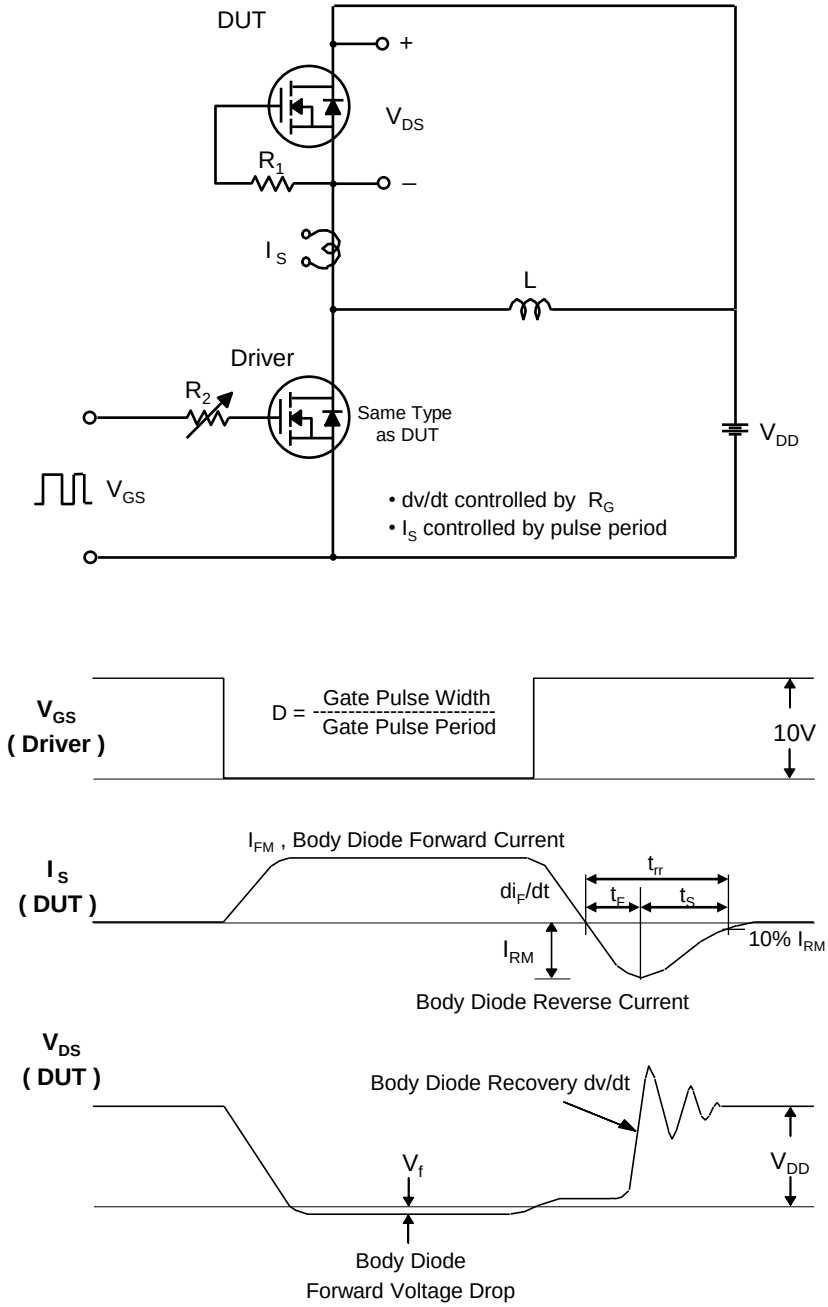
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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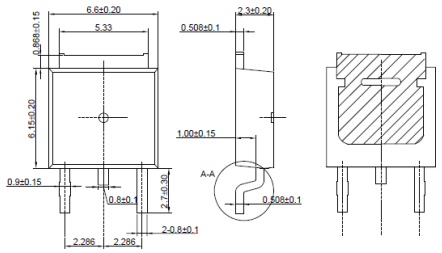
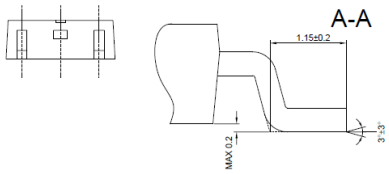
Package Dimension

D-PAK (TO-252A)

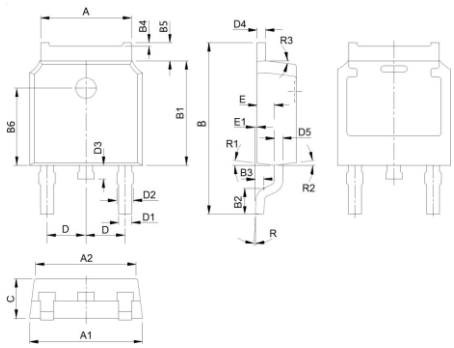
GZSM





1：塑封体为光面RA=0.2
2：未标注公差部分为±0.15mm。

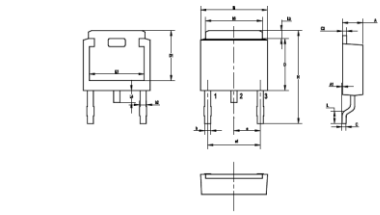
JINTIAN



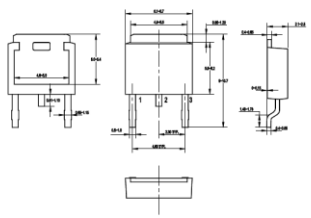
Symbol	Dimensions (mm)	Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A	5.3±0.2	B5	0.95±0.1	D5	0.5±0.08
A1	6.6±0.2	B6	4.5±0.15	E	1.01±0.15
A2	5.8±0.2	C	2.3±0.15	E1	0.1±0.05
B	9.9±0.4	D	2.286(typ.)	R	3°±3°
B1	6.1±0.2	D1	0.76±0.1	R1	7°（typ.）
B2	1.5±0.15	D2	0.91±0.1	R2	7°（typ.）
B3	0.5±0.1	D3	0.8±0.15	R3	7°（typ.）
B4	0.1（typ.）	D4	0.5±0.08		

变更前	
D1	0.62±0.15
D2	0.75±0.15

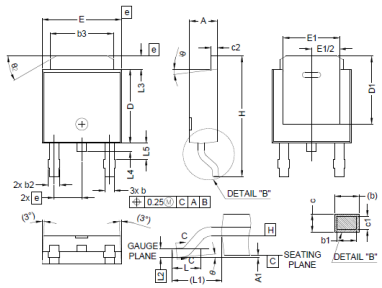
SEMTECH



UNIT	A	A1	b	b2	b3	C	C2	D	D1	E	E1	e	e1	H	L	L3	L4
mm	2.5	0.15	1.0	1.15	5.5	0.65	0.65	6.2	5.4	6.7	5.0	2.30	4.60	10.7	1.78	1.20	1.10
	2.1	0	0.5	0.65	4.9	0.4	0.4	5.6	5.0	6.1	4.6	TYP.	TYP.	9	1.40	0.85	0.51



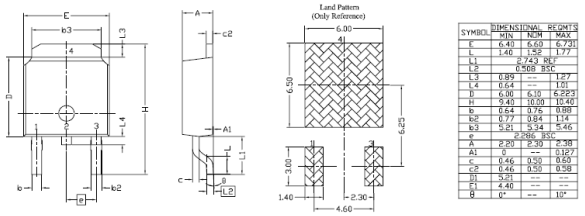
ATX



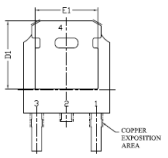
NOTE：
1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3.0 HEAT SINK SIDE FLASH IS MAX. 0.0mm.
4.0 RADIUS ON TERMINAL IS OPTIONAL.

SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.
A	2.18	2.39	E	6.35	6.73	θ1	0°	15°
A1	-	0.13	E1	4.32	-	θ2	25°	35°
b	0.65	0.89	e	2.29 BSC				
b1	0.64	0.79	H	9.94	10.34			
b2	0.76	1.13	L	1.50	1.78			
b3	4.95	5.46	L1	2.74 REF				
c	0.46	0.61	L2	0.51 BSC				
c1	0.41	0.56	L3	0.89	1.27			
c2	0.46	0.60	L4	-	1.02			
D	5.97	6.22	L5	1.14	1.49			
D1	5.21	-	θ	0°	10°			

GEM



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.73
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	---	1.27
L4	0.64	---	1.01
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.75	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	---	0.127
c	0.46	0.50	0.60
c2	0.46	0.50	0.58
D1	5.21	---	---
E1	4.40	---	---
θ	0°	---	10°



Note:
1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
5. Dimension "b" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.10 mm Total In Excess Of "b" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.

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